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(54) **Electron irradiation of power transistors**

(57) A method for reducing storage time and gain parameters in a semiconductor transistor includes the step of subjecting the transistor to electron irradiation of a dosage determined from measurements of the parameters of a test batch of transistors. Reduction of carrier lifetime by proton bombardment and gold doping is mentioned as an alternative to electron irradiation.

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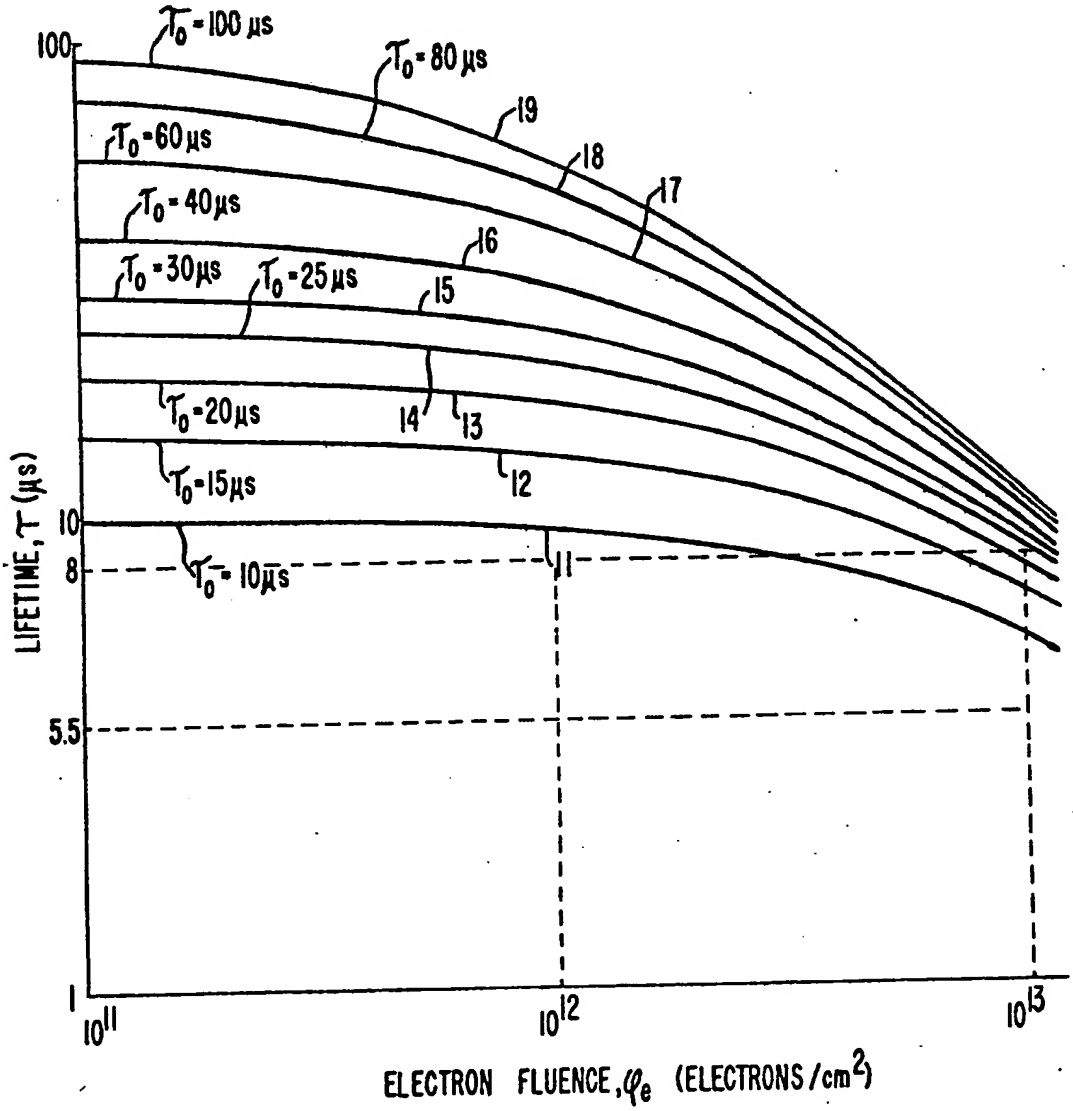

FIG. 1

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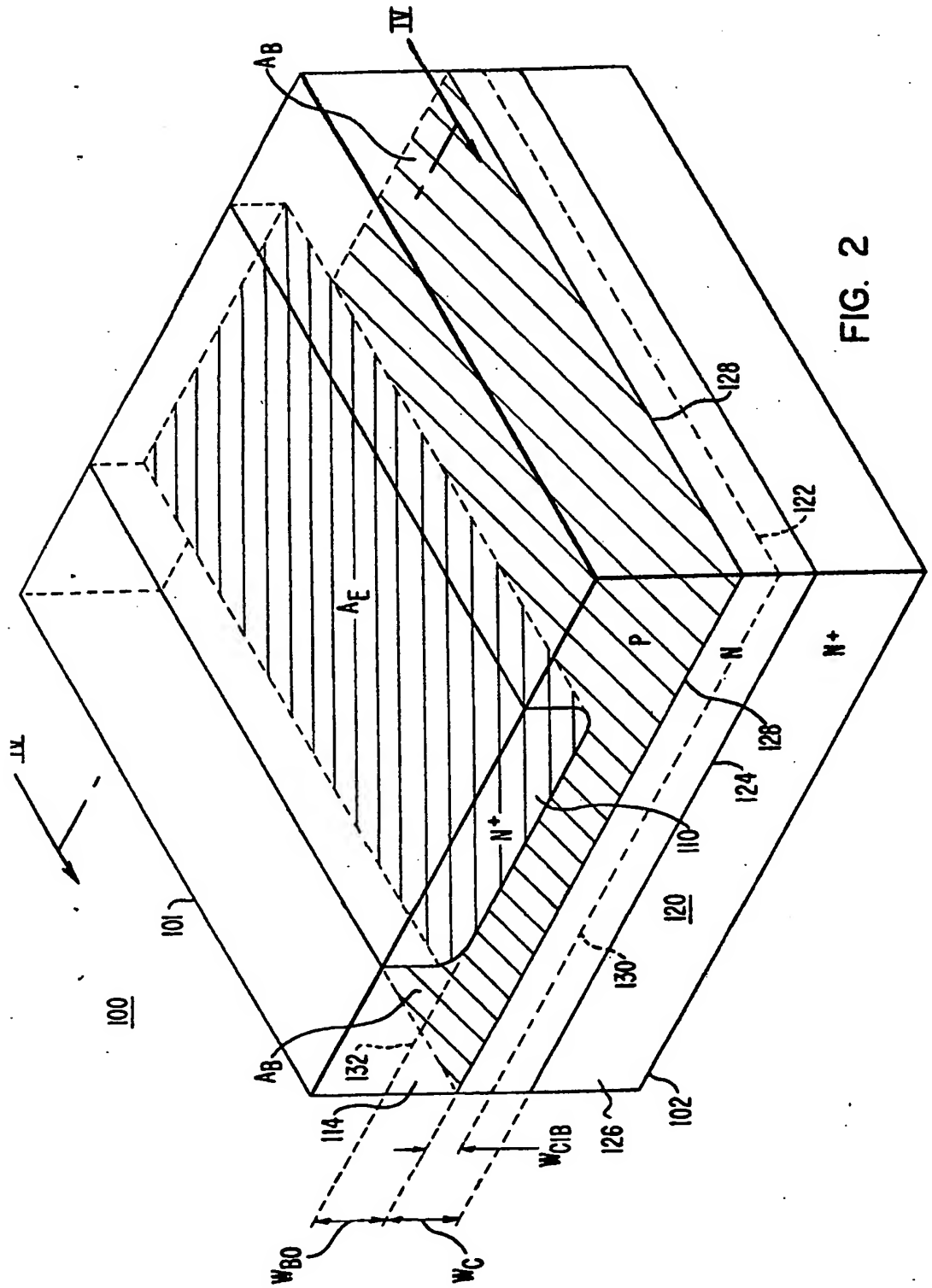

FIG. 2

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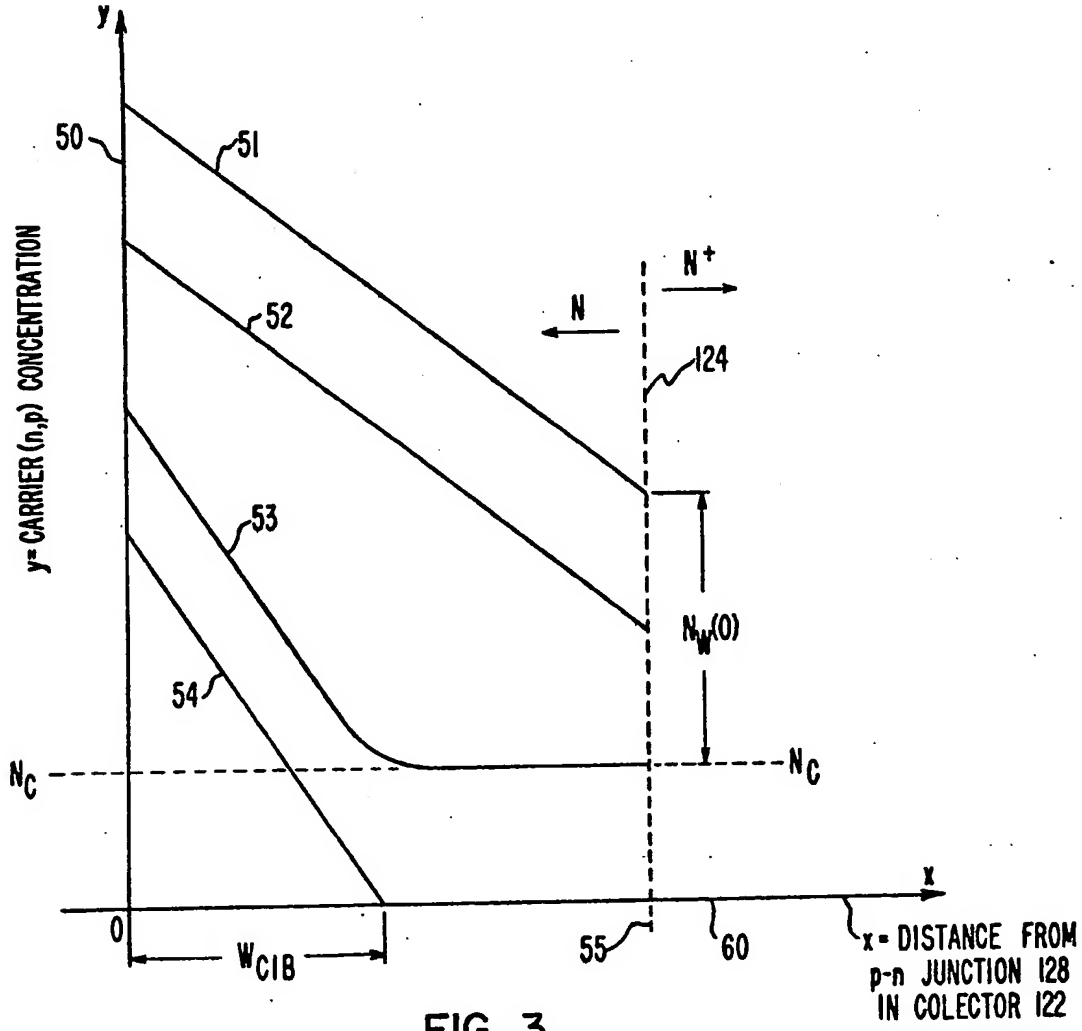

FIG. 3

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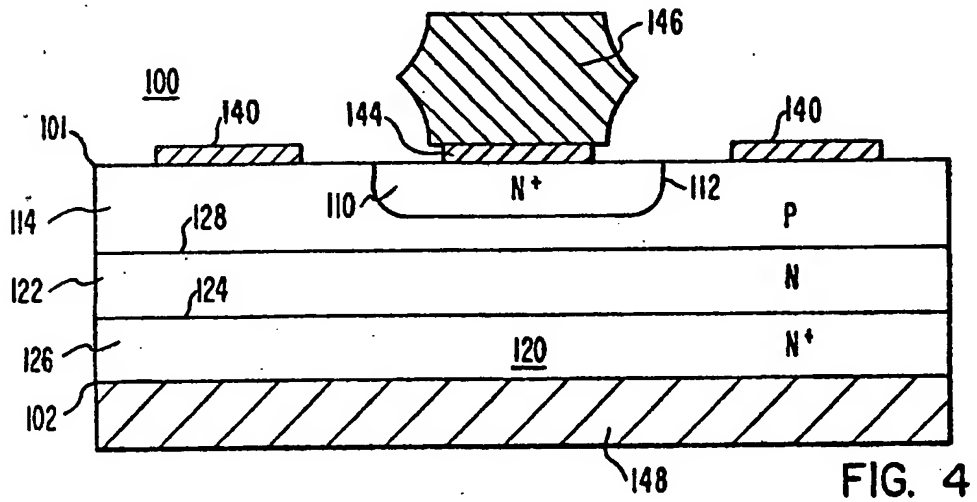

FIG. 4

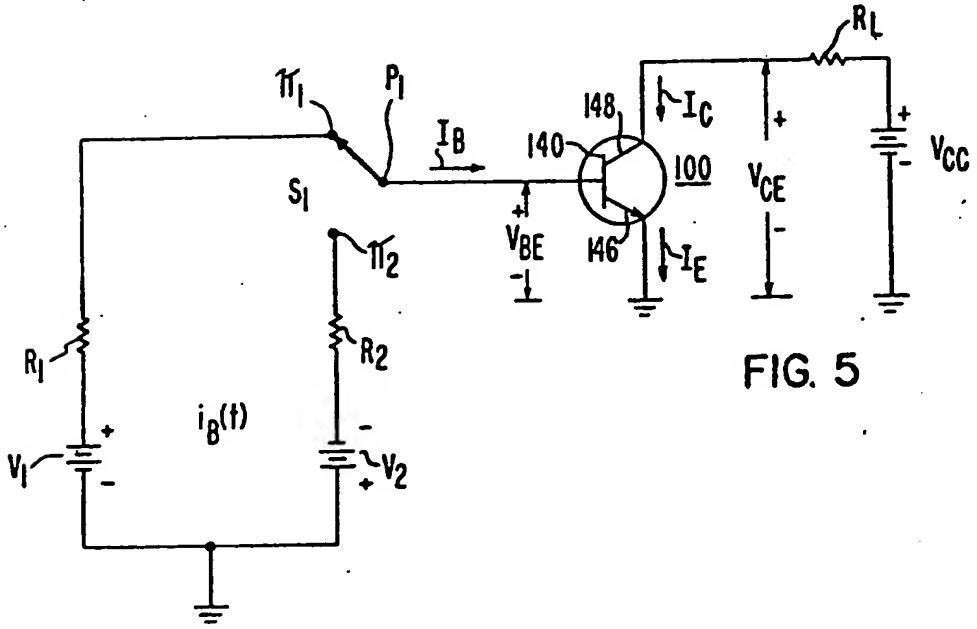

FIG. 5

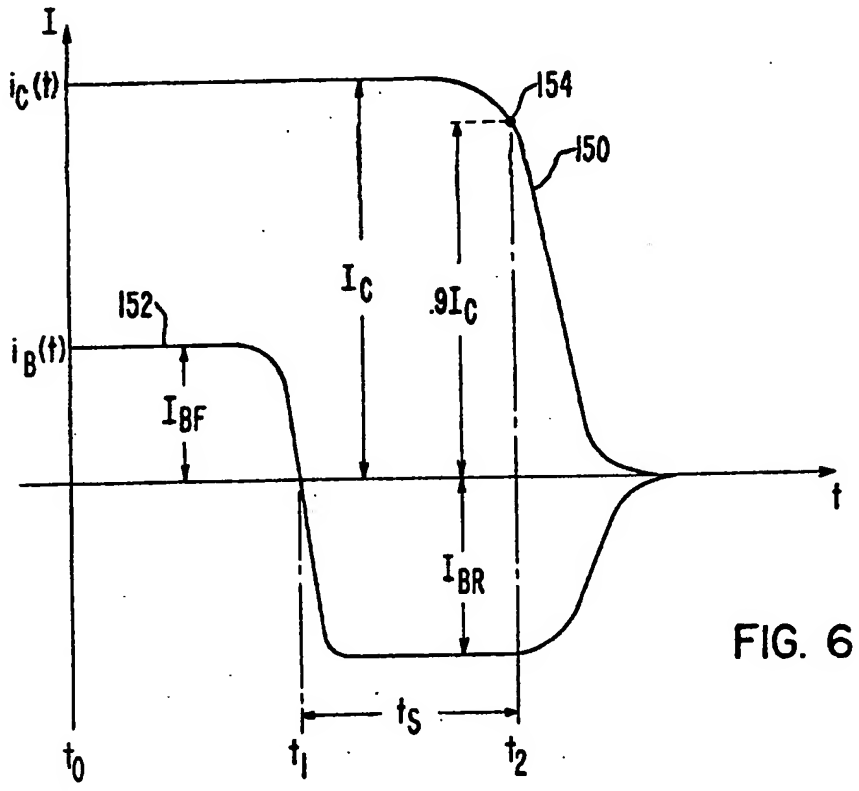
I
$i_C(t)$
154
150
I_C
$.9I_C$
152
$i_B(t)$
I_{BF}
t
I_{BR}
t_S
t_0
t_1
t_2

FIG. 6

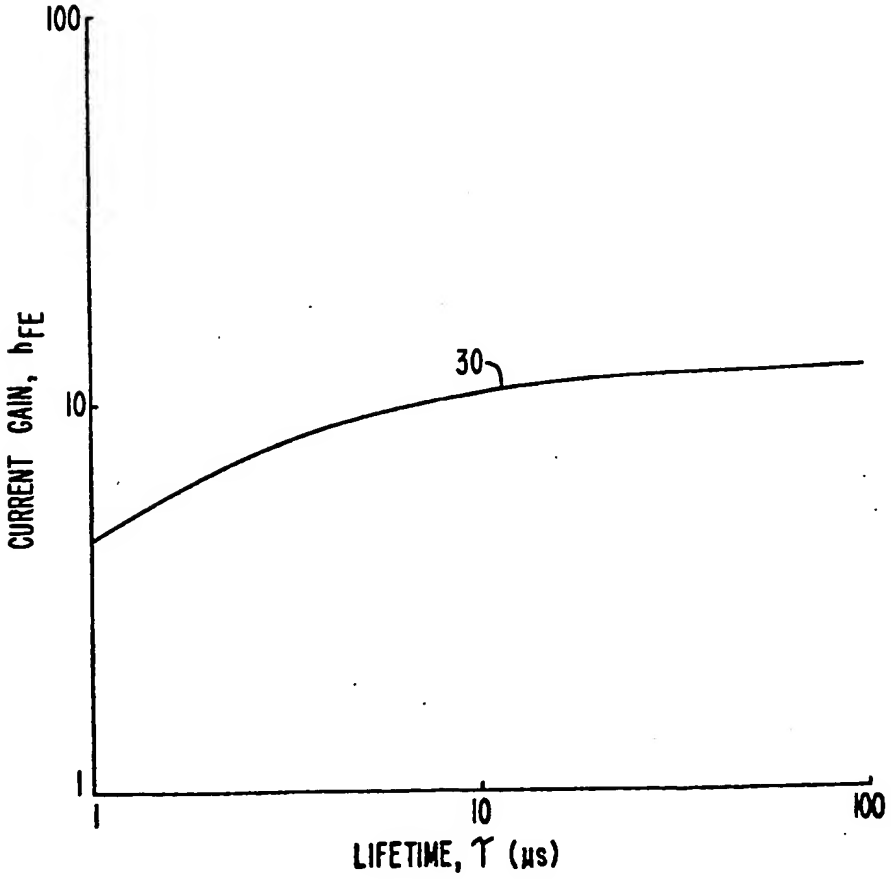
100
CURRENT GAIN, h_{FE}
30
10
1
1
10
100
LIFETIME, τ (μs)

FIG. 7

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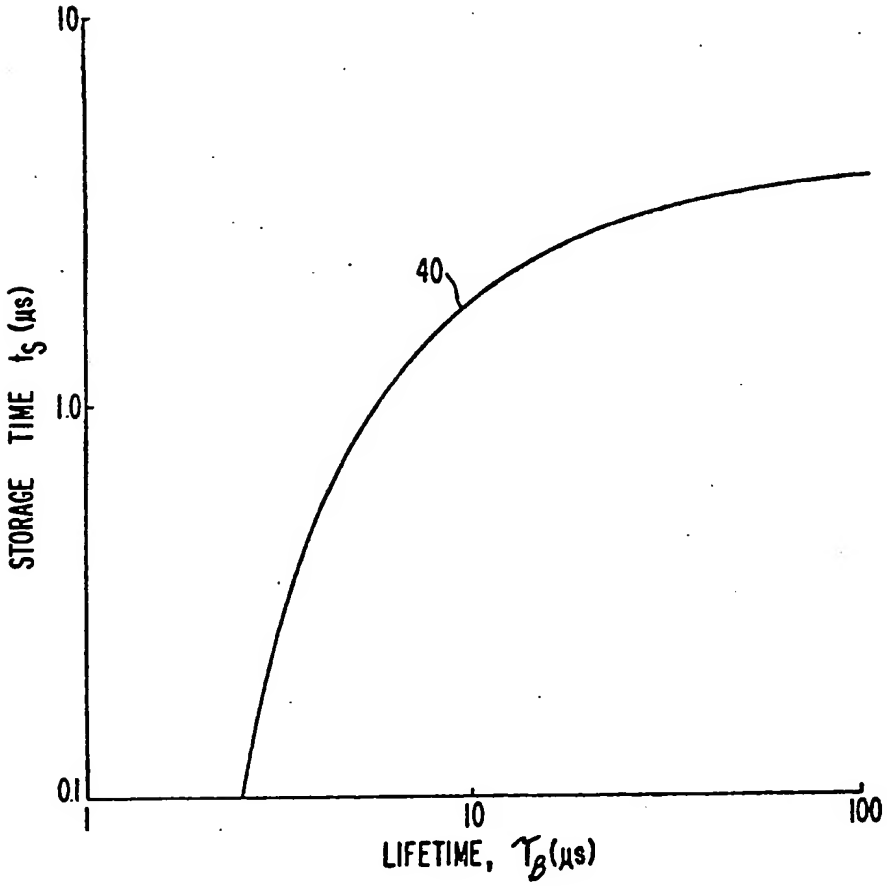

FIG. 8

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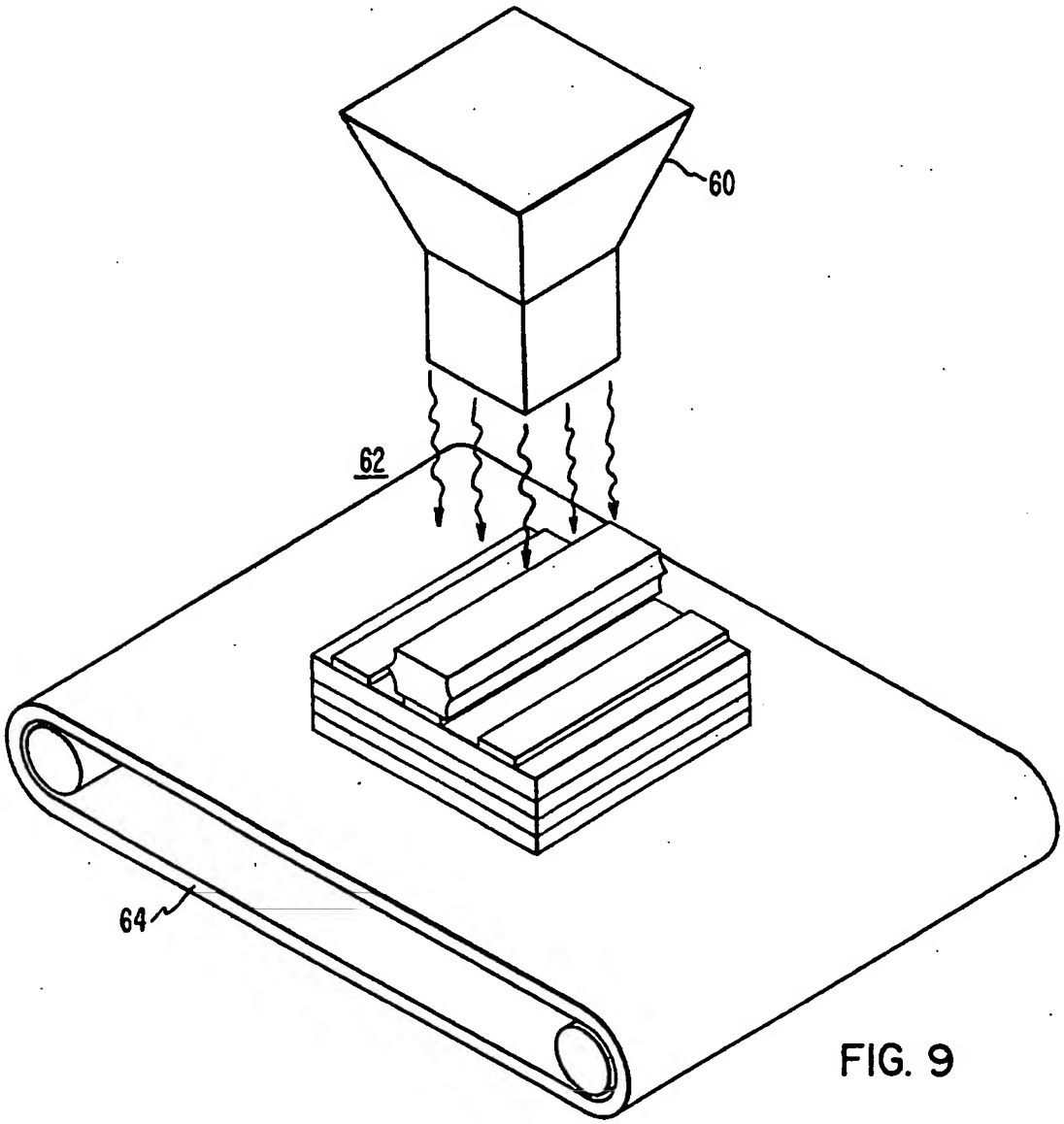

FIG. 9

SPECIFICATION

Electron irradiations of power transistors

This invention relates to the electron irradiating transistors and more particularly power transistors.

Among the important performance parameters included in written specifications for high power semiconductor transistors are storage time t_s, and gain h_{fe}. The storage time parameter t_s is a function of the lifetime τ in the semiconductor material which comprises the metallurgical collector of the transistor. Lifetime τ is that characteristic of a semiconductor region commonly explained as the average time that an excess current carrier exists in a region before it ceases to become an excess current carrier (typically by recombination).

Under present processing methods, it is difficult to control the lifetime in the collectors of power transistors. Typically, τ varies by more than a factor of 2, for example, from 20 μs to 40 μs even in a group of semiconductor wafers that has been exposed to the same processing steps. This variation in τ translates to a variation in storage time t_s. The variation in t_s is undesirable in many applications where circuit adjustments may be required to compensate for device-to-device variations in t_s. In addition, many applications require limits on maximum storage time t_s in conjunction with limits on minimum gain h_{fe}.

It is the object of the invention to change the parameters of transistor by indication.

The invention resides broadly in a method of producing transistors having altered electrical parameters from original transistors, the method comprising the steps of:

characterized by determining an electron radiation dosage in a first test batch of the transistors to meet given gain and storage time characteristics by the measurement of at least one characteristic, of the transistors in the first batch;

positioning a surface of at least one semiconductor device of a second batch of original transistors for exposure to the radiation; and

irradiating said or each semiconductor device of said second batch with electrons having the radiation energy level as determined in the determining step.

According to the teachings of the present invention, the relation in a semiconductor transistor between gain h_{fe} and storage time t_s can be improved to be within limits of predetermined specifications (maximums and minimums). Where the transistor can be characterized by a lifetime τ, a change in such lifetime τ causes a change in the gain h_{fe} and in the storage time t_s according to a predetermined function of lifetime τ. In particular, a reduction in storage time t_s (and gain h_{fe}) can be achieved by irradiating the transistor with a predetermined fluence of radiation, where the level of radiation fluence is proportional to the product of flux intensity and total time of exposure.

More particularly, where the transistor can be characterized by a gain h_{fe}^o and a storage time t_s^o and a particular design application requires minimum gain h_{fe}^{min} and a maximum storage time t_s^{max}, where $h_{fe}^o > h_{fe}^{min}$ and $t_s^o > t_s^{max}$, then, by irradiating the transistor with a predetermined level of electron fluence as determined and specified by the teachings of the method of the present invention, the storage time of the transistor may be reduced to a value less than or equal to t_s^{max} while maintaining a transistor gain value greater than or equal to h_{fe}^{min}. Also, by irradiating the transistor with a predetermined level of electron fluence as determined and specified by the teachings of the present invention, the storage time of the transistor can be minimized while adhering to the constraints of the minimum specified gain h_{fe}^{min}. In general, however, the method of the present invention applies to any process by which it is desired to decrease gain or decrease storage time by a specified amount.

Furthermore, the method can be used for narrowing the range of values of storage time within a group or run of manufactured transistors. A particular run of transistors may be characterized by a range of Δt_s^o of values of storage times ranging from a low of t_s^o to a high of t_s^h. Where a particular design application requires a maximum rang Δt_s^{max} of values of storage times within a run of transistors, then by irradiating the transistor with a level of electron fluence as determined and specified by the teachings of the method of the present invention, the range of values of storage time may be reduced to a range less than or equal to Δt_s^{max} while maintaining a transistor gain value greater than or equal to h_{fe}^{min}.

Figure 1 is a graph of the relation between lifetime and electron fluence;

Figure 2 is an isometric view of a transistor on which the method of the present invention operates;

Figure 3 is a graph of impurity concentration versus distance from the base-collector p-n junction in the collector of the transistor of Figure 2.

Figure 4 is a sectional view of the transistor of Figure 2;

Figure 5 is a circuit for determining the storage time of the transistor of Figures 2 and 4;

Figure 6 is a timing diagram for operating the circuit of Figure 5;

Figure 7 is a graph of the relation between lifetime and current gain;

Figure 8 is a graph of the relation between lifetime and storage time; and

Figure 9 shows particular apparatus for use in the method of the present invention.

Figure 1 is a log-log graph showing the relationship between the effective lifetime τ_e of current carriers in a bipolar transistor and the electron fluence or dosage φ_e to which the transistor is exposed

for various initial lifetimes τ_0. This relationship is well known and shown and explained in an article by P. Rai-Choudbury et al, "Electron Irradiation Induced Recombination Centers In Silicon-Minority Carrier Lifetime Control" in the IEEE Transactions in Electron Devices, Vol. ED-23, No. 8, August 1976.

The relationship can be written:

$$\frac{1}{\tau_e} = \frac{1}{\tau_0} + K' \varphi_e \qquad (1)$$

where:

τ_e is the post irradiation lifetime in seconds (s);
τ_0 is the pre-irradiation lifetime in seconds (s);
K' is the radiation damage coefficient in cm² (e-S);
φ_e is the electron fluence in e/cm².

More directly:

$$\tau_e = \frac{\tau_0}{1 + K' \varphi_e} \qquad (2)$$

where φ_e can be expressed as a function of the product of the time t (in seconds) to which the transistor is exposed to the radiation and the flux density φ_e of the radiation, such that:

$$\varphi_e = f(\varphi_e \cdot t) \qquad (3)$$

Figure 1 includes several curves 11 through 19 plotting the variation in τ_e given the initial lifetime τ_0 for various dosages or fluences φ_e. For example, a curve 11 in Figure 1 plots the variation τ_e for a transistor having an initial lifetime τ_0^{11} of 10 μs. After being exposed to an electron fluence φ_e of 10^{13} electrons/cm², the lifetime τ_e^{11} is 5.50 μs as shown by curve 11. As a further example, a curve 19 in Figure 1 plots the variation in τ_e for a transistor having an initial lifetime τ_0^{19} of 100 μs. After being exposed to an election fluence of φ_e of 10^{13} electrons/cm², the lifetime τ_f^{19} is 10.70 μs as shown by curve 19. Several other curves 12 through 18 as shown in Figure 1 further illustrate the effect of exposing a bipolar transistor having different initial lifetimes to a range of electron fluences. It can be seen from the curves 11 through 19 of Figure 1 that the smaller the initial lifetime τ_0 for a given transistor, the smaller the reduction (τ_0—τ_e) in lifetime.

The following Glossary of Variables and Constants and the Index of Relationships and Equations will be used to facilitate the illustrating of the relationships and equations explaining the method of the present invention.

Glossary of Variables and Constants

A_B = the metallurgical base area (in cm²)
A_E = the metallurgical emitter area (in cm²)
D_B = the effective electron diffusion coefficient in the metallurgical base (dimensionless)
D_C = the high-level majority carrier diffusion coefficient in the collector (in cm²/sec)
D_{CO} = the low-level majority carrier diffusion coefficient in the collector (in cm²/sec)
D_n = the electron diffusion coefficient, generally, in a semiconductor layer
D_n = D_B in the base layer 114
D_n = D_{CO} in the collector layer 120 at low levels
D_n = D_C in the collector layer 120 at high levels
h_B = the recombination parameter for the base (in cm⁴/sec)
h_C = the recombination parameter for the collector (in cm⁴/sec)
h_E = the recombination parameter for the emitter (in cm⁴/sec)
h_{FEO} = the peak current gain (common-emitter configuration) (dimensionless)
$h_{fe}\gamma$ = the emitter frequency limited gain
I_B = the base current (in amps (A))
I_{BF} = the forward base current (in amps (A))
I_{BR} = the reverse base current (in amps (A))
I_C = the collector current (in amps (A))
k = Boltzmann's constant = 8.62×10^{-5} eV/°K
K' = the radiation damage coefficient in cm² (e-S)
N_A = the base acceptor density (in cm^{-3})
N_C = the n-collector donor density (in cm^{-3})
$N_W(0)$ = the excess carrier concentration at the n-n$^+$ junction 124 at t=0 (in cm^{-3}) in classical saturation

q = the electron charge in coulombs = 1.6×10^{-19} coulombs
T = absolute temperature in degrees Kelvin in active region of transistor
t_s = the storage time (in secs)
V_{CE} = the DC collector-to-emitter voltage (in volts)
W_{BO} = the width of the active base (in cm)
W_C = the width of the collector n region (in cm)
W_{CIB} = the width of the current induced base (in cm)
μ_{CO} = the low-level mobility for majority carriers in silicon (in $cm^2/V\text{-}s$)
τ_N = lifetime in n-collector region 122
τ_e = post-irradiation lifetime (in seconds (s))
τ_0 = pre-irradiation lifetime (in seconds (s))
φ_e = the electron fluence (in e/cm^2)

Index of Relationships and Equations

$$B = \frac{W_C}{(h_B+h_C)r_N} + \frac{I_C h_E W_C}{(h_B+h_C)qA_B D_C}$$

$$C = \frac{I_C}{qA_B(h_B+h_C)}\left(\frac{1}{h_{FEO}} + \frac{W_C^2}{4D_C r_N} - \frac{I_{BF}}{I_C}\right) + \frac{I_C^2 h_E}{(h_B+h_C)}\,\frac{(W_C/D_C)^2}{4q^2A_E A_B}$$

$$D_C^* = D_C^2/D_{CO}$$

$$D_{CO} = kt\mu_{CO}/q$$

$$I_0 \frac{q\mu_{C0}V_{CE}N_C A_E}{W_C}$$

$$N_W(O) = \frac{-B}{2} + \sqrt{\frac{B^2}{4} - C}$$

$$Q_O \overset{\Delta}{=} \frac{V_{CE}N_C W_C}{(4kT/q)}$$

$$Q_B = \int_0^{W_{BO}} N_A\, dx$$

$$\frac{Q_B}{D_B} = \int_0^{W_B} \frac{N_A}{D_n}\, dx$$

$$W_{CIB} = W_C\,(1-I_O/I_C)$$

Figure 2 shows an isometric view of a transistor 100 without metallization, which transistor 100 is used in the method of the present invention. The transistor 100 can be referred to in explaining the variables of the above Glossary.

The silicon transistor 100, a top surface 101 and a bottom surface 102 between which is a n-type emitter layer 110 forming a p-n junction 112 with an adjacent p-type base layer 114. A collector 120 includes a n-type layer 122 and a n^+-type layer 126 adjacent thereto which together form a n-n^+ boundary 124. The n-type layer 122 forms a p-n junction 128 with the p-type base layer 114.

The base area A_B is the area covered by the p-n junction 128 and shown by a first cross-hatched area in Figure 2. The emitter area A_E is the area covered essentially by the bottom surface of the n^+ emitter 110, that is, essentially, the area over which current flows across the p-n junction 112. The area A_B is typically approximately two times the size of the area A_E. The width W_{CIB} is the distance in the n-layer 122 from the p-n junction 128 to a line 130 where the excess carrier concentration in the n-layer 122 is zero. The width W_{BO} is a distance in the p-base 114 from the p-n junction 128 to a line 132 tangent to the bottom of the p-n junction 112. The width W_C is the width of the n-type collector region 122.

Measures of the physical properties of the transistor 100 include the diffusion coefficients D_B, D^*_C, and D_{CO}, the recombination parameters h_B, h_C, and h_E, the impurity concentrations N_A and N_C, and the low-level mobility μ_{CO}. The low-level mobility μ_{CO} is a physical property of certain semiconductor materials measured in $cm^2/V\text{-}sec$. The low-level mobility μ_{CO} for majority carriers in silicon is 1300 $cm^2/Vsec$ for a npn transistor. The diffusion coefficients D^*_C and D_{CO} are functions of μ_{CO} as shown in the above Index. The recombination parameters h_B, h_C, and h_E are each measures of the recombination effects of minority carriers in heavily doped regions for the respective regions of the transistor 100. Each of the recombination parameters can be expressed as:

$$h = \frac{D_{eff}}{N_{eff} L_{eff}}$$

where:

D_{eff} = effective diffusion coefficient for minority carriers;
L_{eff} = effective diffusion length for minority carriers; and
n_{eff} = effective majority carrier concentration.

Figure 3 shows a graph of an ordinate axis 50 showing impurity concentration versus an abscissa axis 60 showing distance from the base-collector p-n junction 128 in the collector of the transistor 100 of Figure 2. The graph of Figure 3 includes curves 51 and 52, respectively, showing the n (electron) and p (hole) impurity concentration in the n-collector layer 122 for the forward-biased condition during classical saturation as a function of the distance from the p-n junction 128. Classical saturation describes a condition where the p-n junction 128 is forward-biased everywhere. The slope of the curves 51 and 52 is determined by the current density in the collector 120. The graph of Figure 3 also includes curves 53 and 54, respectively, showing the n and p impurity concentration in the n-collector layer 122 for the forward-biased condition during quasi-saturation as a function of the distance from the p-n junction 128. Quasi-saturation describes a condition where the p-n junction 128 is forward-biased only under the emitter 110, but is reverse-biased elsewhere. A dashed line 55 designates the n-n^+ interface 124. The curve 53 slopes negatively for a distance in the n-collector 122 reflecting a decreasing n (electron) concentration. After a distance equal to the width W_{CIB}, the slope of the curve 53 changes to zero reflecting a constant n (electron) concentration equivalent to the property N_C. The difference in the concentration N_C and the n (electron) impurity concentration at the n-n^+ interface 124 comprises the excess carrier concentration $N_{(W)}(O)$ at the n-n^+ junction 124.

Figure 4 shows a sectional view of the transistor 100 of Figure 2 along the lines IV—IV. Figure 4 shows metallization included on the transistor 100 to provide a complete and working device. A 8 μm thick metal base electrode 140 is disposed on the exposed surface of base layer 114 and can be comprised of any conductive metal, but aluminium is preferred. A 8μm thick metal emitter electrode 144 is disposed on the exposed surface of the emitter layer 110 and can be of the same composition as the electrode 140. A 6 mil thick piece 146 of molybdenum is disposed upon the emitter electrode 144 and a 30 mil thick 148 piece of molybdenum is disposed on the exposed surface of the n^+ layer 126 for forming a collector electrode.

Figure 5 shows a circuit for determining the storage time t_s of the transistor 100. In Figure 5, like reference characters designate corresponding parts in the preceding figures. A resistor R_L is coupled between a power supply V_{cc} and the collector electrode 148. The emitter electrode 146 is coupled to ground and the base emitter 140 is coupled to a source of current $i_B(t)$. The source of current $i_B(t)$ includes power supplies V_1 and V_2 each having a positive and a negative terminal and includes resistors R_1 and R_2. The source of current $i_B(t)$ also includes a single-pole-double-throw switch S_1 having a pole P_1 and terminals π_1 and π_2. The negative terminal of the power supply V_1 is coupled to ground and the positive terminal thereof is coupled to one end of the resistor R_1. The other end of the resistor R_1 is

coupled to the switch terminal π_1. The positive terminal of the power supply V_2 is coupled to ground and the negative terminal thereof is coupled to one end of the resistor R_2. The other end of the resistor R_2 is coupled to the switch terminal π_2. The storage time is referred to as that period of time required for the collector current I_C to decrease to $.9I_C$ after a reverse-bias current I_{BR} has been supplied to the transistor 100. Figure 6 shows a timing diagram for determining the storage time t_s for the transistor 100. Curves 150 and 152 show the instantaneous values $i_C(t)$ and $i_B(t)$ of the collector current and the base current, respectively. At a time t_0, a forward-biasing base current I_{BF} is supplied to the base electrode 140 of the transistor 100 as shown by curve 152 of Figure 6 at time t_0 resulting in a current I_C in the collector electrode 148. At a time t_1, the reverse-biasing base current I_{BR} is substituted for the base current I_{BF} as shown by curve 152 in Figure 6 at time t_1. The collector current I_C will decrease to $.9I_C$ at a time t_2. The period of time between time t_1 and time t_2 is the storage time t_s.

It has been determined that a relationship exists between current gain h_{fe} and collector lifetime τ_N. The relationship is illustrated by curve 30 in Figure 7. The equation from which the curve 30 is derived or plotted is:

$$h_{fe} = f(\tau_N) = h_{fe}\gamma/(1 + \delta) \quad (4)$$

where:

$$h_{fe}\gamma = \frac{h_{fe0}}{1 + \frac{Q_O D_B}{Q_B D_C^*}\left(\frac{I_C^2 + I_O^2}{I_O I_C} - 2\right)} \quad (5)$$

and

$$\delta \triangleq h_{fe}\gamma\,(W_{CIB}^2/(4D_C\tau_N) \quad (6)$$

where the variable, constants, and relationships expressed in equations (4), (5) and (6) are detailed in the above Glossary of Variables and Constants and the Index of Relationships and Equations. More directly, the relationship between gain h_{fe}, electron fluence ϕ_e and τ_0 can be written:

$$h_{fe} = f(\phi_e) = \frac{h_{fe}\gamma}{1 + \frac{W_{CIB}^2 h_{fe}\gamma(1 + K'\phi_e)}{4D_C\tau_N}} \quad (7)$$

For the curve 30 plotted in Figure 7, the variables of equation (7) have the following values:

$I_C = 50$ A

$V_{CE} = 2.5$ V

$h_E = 2 \times 10^{-14}$ cm^{-4}/S

$A_E = 1$ cm^2

$W_C = 50 \times 10^{-4}$ cm

$N_C = 1.4 \times 10^{14}$ cm^{-3}

$h_{fe0} = 25$

It has also been determined that a relationship exists between storage time t_s in a transistor and the effective base transit lifetime τ_B in the same transistor. Figure 8 shows a graph containing a curve

40 which plots the relationship of t_s vs.τ_B in a transistor. The equation from which the curve 40 is derived is:

$$t_s = f(\tau_B) = \tau_B \ln \left[1 + \frac{N_W(O)W_C(A_B/A_E)}{\frac{N_W(O)W_C}{2} \quad \frac{I_{BR}\tau_B}{gA_E}} \right] \tag{8}$$

and where

$$\tau_B = \frac{I_C}{I_{BF}} \left[\frac{W_C^2}{4D_C} + \frac{qA_B}{I_C} N_W(O)W_C \right] \tag{9}$$

where the variables, constants, and relationships expressed in equation (8) are detailed in the above Glossary of Variables and Constants and the Index of Relationships and Equations.

More directly, equation (8) can be expressed as a function of electron fluence φ_e and initial lifetime τ_N:

$$t_s = \frac{\tau_N}{1+\tau_N K'\dot{\varphi}_e} \ln \frac{(1+N_W(O)W_C(A_B/A_E))(1+\tau_N K'\dot{\varphi}_e)}{\frac{I_C W_C^2}{4qD_C A_E}(1+\tau_N K'\dot{\varphi}_e) + \frac{I_{BR}}{qA_E}\tau_N} \tag{10}$$

For the curve 40 plotted in Figure 8, the variables of equation (9) have the following values:

$I_C = 50A$

$I_{BF} = I_{BR} = 4A$

$h_E = 2 \times 10^{-14}\ cm^{-4}/S$

$h_B + h_C = 2h_E$

$A_E = 1\ cm^2$

$W_C = 50 \times 10^{-4}\ cm$

$N_C = 1.4 \times 10^{14}\ cm^{-3}$

From equation (1) and the curves 11 through 19 of Figure 1, a specified dosage φ_e of radiation can be used to decrease lifetime τ_N and, in turn, lifetime τ_N can be used to compute the relationship between radiation dosage φ_e and gain h_{fe} from equation (7) and Figure 7 and between radiation dosage φ_e and storage time t_s from equation (9) and Figure 8.

The following example will serve to illustrate and clarify the method of the present invention:

EXAMPLE

A particular design application requires or specifies:

$h_{fe}^o \geq 10$ (minimum gain)
$t_s^o \leq 2\ \mu s$ (maximum storage time); and

a particular manufacturing process produces a group or run of transistors having a lifetime τ_0 where:

$$\tau_0 = 40\ \mu s.$$

From equations (7) and (9) and curves 30 and 40,

$h^o_{fe} = 11.9$ (gain of the group of transistors after manufacturing process);
$t^o_s = 3.3\ \mu s$ (storage time of transistors after manufacturing process);

h^o_{fe} exceeds the specified or required gain d^d_{fe} but t^o_s is greater than the specified storage time t^o_s and does not meet the design requirement. Assuming that the run of transistors is desired to have performance characteristics such that the gain $h^{\varphi e}_{fe}$ after irradiation is as large as possible while reducing the storage time $t^{\varphi e}_s$ after irradiation to meet the design requirement ($t^{\varphi e}_s \leq t^d_s$), the proper dosage φ_e can be determined or computed using curves 16 and 40 and the equations (1) and equations (8) or (9), respectively, from which the curves 16 and 40 are derived. For a storage time $t^{\varphi e}_s$ after irradiation of 2 μs, a lifetime τ_e after irradiation is required where:

$$\tau_e = 11\ \mu s,$$

which relationship is obtained from curve 40 of Figure 8. In Figure 1, the curve 16 plots the relationship between lifetime τ_e after irradiation and radiation dosage φ_e for a transistor having an initial lifetime τ^{40}_0 where:

$$\tau^{40}_0 = 40\ \mu s.$$

Following the curve 16 of Figure 1, it can be observed that the proper dosage φ_e of radiation required to cause a lifetime τ_e of 10 μs is approximately 8×10^{12} electrons/cm^2 which, in turn, causes a storage time $t^{\varphi e}_s$ after irradiation of 2 μs. From the curve 30 in Figure 7, it can be observed that for a lifetime τ_e of 11 μs, the gain for a transistor in run of this Example (1) is reduced from 11.9 to $h^{\varphi e}_{fe}$ of 10.6 which gain $h^{\varphi e}_{fe}$ after irradiation is the largest gain $h^{\varphi e}_{fe}$ possible given a storage time $t^{\varphi e}_s \leq 2\ \mu s$ as required by the design specification and given an initial gain h^o_{fe} of 11.9.

Continuing with the design specifications and transistor performance characteristics of this Example (1), and assuming that the run of transistors of this Example (1) is desired to have performance characteristics such that the storage time $t^{\varphi e}_s$ after irradiation is as small as possible while maintaining the gain $h^{\varphi e}_{fe}$ after irradiation greater or equal to the design specified gain h^d_{fe}, the proper dosage φ_e of radiation can be determined using curves 16 and 40 and the equations (1) and (7), respectively from which the curves 16 and 30 are derived. For a gain $h^{\varphi e}_{fe}$ after irradiation of 10, a lifetime τ_e after irradiation is required where:

$$\tau_e = 8\ \mu s,$$

which relationship is obtained from the curve 30 of Figure 7. Following the curve 16, it can be observed that the appropriate dosage φ_e of radiation required to cause a lifetime τ_e of 8 μs is approximately 1.015×10^{13} e/cm^2, which, in turn, causes a gain $h^{\varphi e}_{fe}$ after irradiation of 10. From the curve 40 in Figure 8, it can be observed that for a lifetime τ_e of 8μs, the storage time for a transistor in the run of this Example (1) is reduced from 3.3 μs to a storage time $t^{\varphi e}_s$ for a transistor in the run of this Example (1) given a gain $h^{\varphi e}_{fe} \geq 10$ and given the initial conditions $h^o_{fe} = 11.9$ and $t^o_s = 3.3\ \mu s$.

Figure 9 shows a preferred method of irradiating the transistor 100 of Figures 2, 4 and 5. The apparatus of Figure 9 includes a radiation means 60 for producing electron radiation 62, the electrons of said radiation preferably having an energy level of approximately 2 MeV, but in any event the energy level of said radiation should be sufficient to alter the recombination lifetime in the collector layer 122. A conveyor belt 64, on which the transistor 100 lies, is situated under the radiation means 60. The transistor 100 should be oriented such that the top surface 101 is first exposed to the radiation 62. The belt 64 should be moving at a predetermined speed such that the total time that the transistor 100 is exposed is sufficient to give the predetermined electron fluence exposure.

While the invention has been described in its preferred embodiment, it is to be understood that the application described is not intended to be a limitation and that other applications are possible within the purview of the appended claims without departing from the true scope and spirit of the invention in its broader aspects.

It will be appreciated by those skilled in the art that the method of the present invention may be carried out in various ways and may take various forms and applications other than the illustrative application heretofore described. For example, the method of the present invention can be applied where a particular design application requires a storage time t^d_s, where:

$$t^d_s = t_{so} \pm \Delta t^d_e$$

t_{so} = specified storage time

where:

$$t_e^d \leq 1\ \mu s$$

and a particular manufacturing process produces a group or run of transistors having a range of lifetimes τ_0 where it is determined, for example, by statistical analysis that the variation storage times of the manufactured transistors exceeds the required variation.

In addition, the method of the present invention applies to pnp-type transistors so that, where reference in the foregoing specification is made to acceptors and donors, donors and acceptors would be substituted, respectively, where a pnp-type transistor is being used. Further, where reference in the foregoing specification is made to electrons and holes, holes and electrons would be substituted, respectively, where a pnp-type transistor is being used.

Important note should be taken that although a means of electron irradiation is used to explain the method of the present invention, such means is intended to be illustrative only and not to be a limitation. Other conventional means of radiation (e.g., proton) are contemplated and, indeed, the scope of the present invention includes any means of changing lifetime in the semiconductor transistor, for example, gold doping.

Since still other applications are possible, it is to be understood that the scope of the method of the present invention is not limited by the details of the foregoing description and illustrative example, but will be defined in the following claims.

CLAIMS

1. A method of producing transistors having altered electrical parameters from original transistors, the method comprising the steps of:

characterized by determining an electron radiation dosage in a first test batch of the transistors to meet given gain and storage time characteristics by the measurement of at least one characteristic, of the transistors in the first batch;

positioning a surface of at least one semiconductor device of a second batch of original transistors for exposure to the radiation; and

irradiating said or each semiconductor device of said second batch with electrons having the radiation energy level as determined in the determining step.

2. A method according to claim 1 characterized in that the determining of the energy level comprises the measurement of the gain and storage time of the irradiated transistors of said first test batch.

3. A method according to claim 1 or 2 characterized in that the radiation is determined by ascertaining the emitter efficiently limited gain, the width of the current induced base, the pre-irradiation lifetime, the radiation damage coefficient and the high-level majority carrier diffusion coefficient in the collector, by dividing the emitter efficiency limited gain by one plus a first quantity being the quotient of the base width times the limited gain times a second quantity, one plus the pre-irradiation lifetime times the radiation damage coefficient times the electron fluence, over four times the majority diffusion coefficient times the pre-irradiation lifetime.

4. A method according to any of the preceding claims characterized in that the storage time is determined by the pre-irradiation lifetime divided by a fourth quantity being one plus the lifetime times the radiation damage coefficient times the electron fluence, said fourth quantity multiplied by the natural logarithm of a fifth quantity being a quotient between a sixth and a seventh quantity, said sixth quantity comprising an eighth quantity being one plus the excess carrier concentration in saturation, times the width of the collector region times the quotient of the metallurgical base area over the metallurgical emitter area, the eighth quantity times one plus the product of the pre-irradiation lifetime, the radiation damage coefficient and the electron fluence, said seventh quantity comprising a ninth quantity being the quotient of a given collector current times the width of the collector squared over four times the electron charge times the collector high-level majority carrier diffusion coefficient times the metallurgical emitter area, the immediately aforesaid quotient times one plus the product of the pre-irradiation lifetime and the radiation damage coefficient and the electron fluence, said seventh quantity further comprising said ninth quantity plus the product of the reverse base current and the pre-irradiation lifetime divided by the electron charge times the metallurgical emitter area.

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